MALLA REDDY COLLEGE OF ENGINEERING &TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

(Affiliated to JNTU, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade, ISO 9001:2008 Certified)

Maisammaguda, Dhulapally, Secunderabad – 500100.

DEPARTMENT OF
ELECTRONICS & COMMUNICATION ENGINEERING

III B.TECH I SEMESTER QUESTION BANK

(2019 – 20)

INDEX

R17A0408

IC APPLICATIONS

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester supplementary Examinations

IC Applications

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: Answer one question from each section

SECTION-I

1 a) Explain the operation of non-inverting Op-amp and derive the expression for output voltage? [10M]

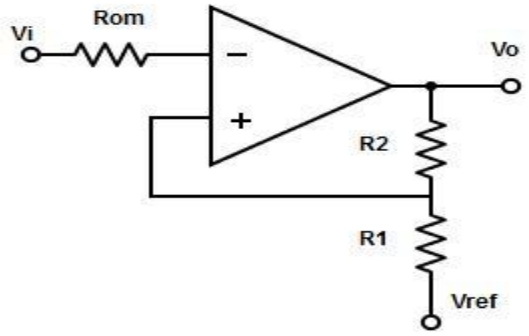
b) If the differential voltage gain and common mode voltage gain of a differential amplifier are 48dB and 2 dB respectively then calculate the CMRR. [4M]

(OR)

2 a)Explain the Working of Instrumentation Amplifier with suitable diagram. [7M]

b) Calculate the hysteresis voltage for the schmitt trigger from the given specification:

R_2 **=56kΩ , R**$_1$ **= 100Ω ,V**$_{ref}$ = 0v & V_{sat} = ±14v. [7M]



SECTION-I

4. a) Draw the circuit and explain the operation of 1^{st} order LPF Butterworth filter. [7M]
   b) Design a wide band reject filter having f_H= 400 Hz and f_L= 2KHz with a pass band gain of 2. [7M]

(OR)

5. a) Draw the block diagram of Astable multivibrator operations using IC 555 and derive its time constant. [10M]
   b) Write the applications of PLL 565.[4M]

SECTION-II

6. Explain the operation of successive approximation ADC and discuss its merits and de-merits. [14M]

(OR)

7. Explain the R-2R ladder DAC and Inverted R-2R DAC with neat diagram.[14M]

SECTION-III

8. Design binary to Gray code converter using gates.[14M]

(OR)

9. Design a 32 to 1 multiplexer using four 74×151 multiplexers and 74×139 decoder .[14M]

SECTION-IV

10. Explain Decade Binary Counter. [14M]

(OR)

11. a) Explain the functional behavior of Static RAM cell? Show the internal structure of 8X4 static RAM. [10M]
    b) List out the applications of ROM. [4M]

R15

Code No: **R17A0408**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Regular Examinations

IC Applications

(ECE)

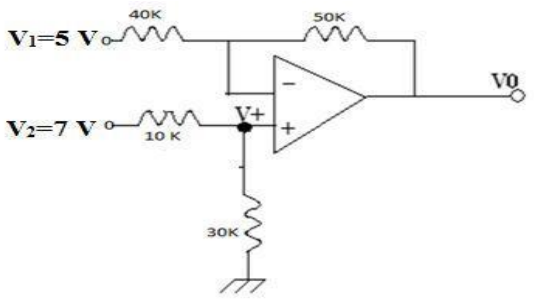
Roll No										

Time: 3 hours **Max. Marks: 70**

Note: Answer one question from each section.

SECTION – I

1. (a) Using IC7812, design a circuit to generate +5V output. [7M]
   (b) An adder-subtractor circuit designed using operational amplifier is shown below. Determine the output voltage for the given combinations of the inputs. Assume ideal op-amp. [7M]



(OR)

2.(a) Define the term CMRR, Input offset voltage, input offset current, input bias current, out offset voltage with reference to OPAMPs. [7]

(b) Explain the operation of Schmitt trigger with the help of neat sketches. [7]

SECTION – II

3. (a) Design first order Butterworth low pass filter with high cutoff frequency f_H = 1.59 KHz and pass band gain of 10. Compute the gain at cutoff frequency. Plot the frequency response of the designed filter. [7]

   (b) Compare and contrast, minimum any four features of active filters with passive filters. [7]

OR

4. (a) Explain mono-stable multi vibrator using IC 555 [7]

   (b) If R_A = 6.8 K, R_B = 3.3 K, C = 0.1 μF in a 555 based astable multivibrator, calculate the following [7]

   1) t_{high}
   2) t_{low} 3) Free running frequency 4) Duty cycle

SECTION – III

5. (a) For a Digital to Analog converter (DAC) with 0-10 Volts range, calculate the values of LSB, MSB and output voltage for a digital input of 1010. Estimate the DAC's Quantization error. [7]

   b) Design a R-2R network for DAC [7]

(OR)

6. (a) Explain Successive approximation ADC with conversion process [7]

   (b) Explain dual slope ADC with neat diagram [7]

SECTION – IV

7. (a)Draw the 4 bit Parallel Adder (74LS283) and logic diagram. Explain its functioning with one example. [7]

   (b) What are decoders? Draw the pin diagram of and logic diagram of 4X16 Decoder (74HC154). [7]

(OR)

8. (a) Design binary to Gray code converter . [10]
   (b) Explain MUX [4]

SECTION – V

9. Design a Modulo-10 counter using any flip flop. [14]

(OR)

10. Design a conversion circuit to convert an S-R Flip Flop to J-K Flip Flop? [14]

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MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech III year – I Semester Examinations,

Model Paper-1

IC Applications

Time: 3 hours **Max. Marks: 70**

SECTION-I

1. Draw and explain the waveforms of inverting and non-inverting Comparator (14M)

OR

2. Explain the working of an ideal & practical differentiator (14M)

SECTION-II

3 With a neat diagram explain about triangular wave generator and derive the frequency of Oscillation (14M)

OR

4 With a neat diagram explain about sawtooth wave form generator (14M)

SECTION-III

5 Explain the operation of parallel comparator type ADC with the help of a neat diagram (14M)

OR

6 Explain the operation of a Successive approximation type analog to digital converter (14M)

SECTION-IV

7 Explain Binary to Gray and Gray to Binary code conversion with one example each (14M)

OR

8 Explain the IC interfacing between TTL and CMOS

SECTION-V

9 Draw the D filp-flop and T flip-flop and explain the operation with truth table (14M)

OR

10. (a) Draw the JK flip-flop and explain it's operation with truth table (7M)

(b) Explain D flip-flop with help of diagram and truth table (7M)

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech III year – I Semester Examinations, Model Paper-2

IC Applications

Time: 3 hours **Max. Marks: 70**

SECTION-I

1 Draw and explain the operation of an op-amp as an integrator (14M)

OR

2 Explain the modes of operation of an op-amp (14M)

SECTION-II

3 How a symmetrical wave form generator can be constructed using 555 timer (14M)

OR

4 If R_A **= 6.8 KΩ,** R_B **= 3.3 KΩ, C = 0.1μF in 555 Astable Multivibrator. Calculate**

i) t_{high} ii) t_{Low} iii) Free running frequency iv) Duty Cycle (14M)

SECTION-II

5 a) Calculate the number of bits required to represent a full scale voltage of 10V with a Resolution of 5mV approximately (7M)

b) List out different types of A/D converters (7M)

OR

6 Explain the operation of weighted resistor DAC with neat circuit diagram (14M)

7 a) Explain 4 bit parallel adder (7M)

b) Explain 4-bit magnitude comparator (7M)

OR

8 Explain Decoders (14M)

9 Explain 3 bit asynchronous counter with neat diagram (14M)

OR

10 a) Assume the propagation delay of each flip-flop is 12 ns. What is the total propagation delay and the max clock frequency of a 3 bit asynchronous Binary counter (7M)

b) Explain the 2-bit synchronous binary counter (7M)

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech III year – I Semester Examinations,

IC Applications

Time: 3 hours **Max. Marks: 70**

1 Explain inverting & non-inverting comparator (14M)

OR

2 a)Explain the Schmitt trigger (7M)

b) Explain the features of 723 regulators (7M)

3 Draw and explain the frequency response of all filters based on frequency range (14M)

OR

4 a) Write the design steps for 1^{st} order LPF (7M)

b) Explain the frequency scaling (7M)

5 Explain about ladder type DAC with neat diagram (14M)

OR

6 What is the drawback of weighted resistor DAC. Write down the method to Overcome this drawback (14M)

7 Explain Encoders (14M)

OR

8 Explain an 8-input Data Selector / Multiplexer (14M)

9 Explain the synchronous BCD decade counter (14M)

OR

10 What is the shift register? Explain different kinds of shift Register (14M)

MALLA REDDY COLLEGE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

B.Tech III year – I Semester Examinations,

IC Applications

Time: 3 hours **Max. Marks: 70**

1 Explain three terminal voltage regulators	(14M)
OR	
2 Explain the inverting and non-inverting AC amplifier	(14M)
3 Explain the functional diagram of IC 555 timer	(14M)
OR	
4 Explain the monostable multivibrator operation and derive it's pulse width	(14M)
5 Explain the DAC and ADC specifications.	(14M)
OR	
6 Explain the counter type ADC	(14M)
7 a) Explain 4 line to 16 line demultiplexer	(7M)
b) Explain parity generators/checkers	(7M)
OR	
8 Use 74HC85 comparators to compare magnitudes of two 16 bit numbers. Show the comparators with proper interconnections	(14M)
9 Explain asynchronous Decade counters	(14M)
OR	
10Explain ROM and it's types and RAM and it's types	(14M)

R17A0409

ANALOG COMMUNICATIONS

R17

Code No: **R17A0409**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Examinations

Analog Communications

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

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SECTION – I

1. a) Explain how an amplitude modulated signal can be detected using a square law detector.[10M]
   b) An AM transmitter radiates 50W power when carrier is modulated and μ=0.707. Determine i) carrier power ii) modulation efficiency [4M]

(OR)

2. a) Explain how a DSBSC signal is represented in the time and frequency domain[7M]
   b) Explain how a DSBSC signal is generated using a balanced modulator.[7M]

SECTION – II

3. a) Explain how a SSBSC signal is generated using a filter method.[7M]
   b) Compare different amplitude modulation techniques. [7M]

(OR)

4. a) Explain the generation of VSBSC signal [7M]
   b) What are the applications of different amplitude modulation systems.[7M]

SECTION – III

5. a) Derive the expression for single tone frequency modulated signal.[7M]]
   b) A 100 M Hz carrier is frequency modulated by a sinusoidal signal of amplitude 20V and frequency 100K Hz .The frequency sensitivity of the modulator is 25K Hz/volt. Determine i) frequency deviation ii) modulation index (β) iii) bandwidth [7M]

(OR)

6. a) Explain about pre emphasis and de emphasis in FM systems [8M]
   b) Compare AM & FM [6M]

SECTION – IV

7. a)Define i) Noise bandwidth Ii) Noise figure [4M]
   b) Derive the expression of figure of merit for Amplitude modulated system.[10M]

(OR)

8. a) Derive the expression of figure of merit for DSBSC system.[7M]
   b) Derive the expression of figure of merit for frequency modulated system [7M]

SECTION – V

9. a) Explain the characteristics of a radio receiver.[6M]
   b) Explain the operation of Tuned radio frequency (TRF) receiver with the block diagram and mention its advantages and disadvantages. [8M]

(OR)

10. Explain the generation and de modulation of PAM signals.[14M]

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester Regular Examinations

Analog Communications

(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE

Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

******

SECTION – I

1. a) Explain how an amplitude modulated signal can be generated using a switching modulator.[8M]

   b) Consider an AM signal $s(t)=20(1+0.9\cos 2\pi 10^4 t)\cos 2\pi 10^6 t$.The signal is radiated into free space using an antenna having resistance of 5Ω. Calculate i) Power ii) Bandwidth iii) modulation efficiency [6M]

(OR)

2. a) Explain how a DSBSC signal is represented in the time and frequency domain,[7M]
   b) Explain how a DSBSC signal is detected using a coherent detector.[7M]

SECTION – II

3. a) Explain how a SSBSC signal is represented in time and frequency domain.[7M]
   b) Explain how a SSBSC signal is generated using phase shift method. [7M]

(OR)

4. a) Explain the detection of VSBSC signal [8M]
   b) What are the applications of different amplitude modulation systems. [6M]

SECTION – III

5. a) Derive the expression for Narrow band frequency modulated signal.[10M]]
   b) Consider an FM signal $s(t)=10\cos(2\pi\ 10^6 t+8\sin 4\pi\ 10^3 t)$.Determine i)Modulation index ii) frequency deviation iii) power iv) bandwidth [4M]

(OR)

6. a) Explain how a frequency modulated signal is generated using varactor diode [7M]
   b) Explain how a FM signal is demodulated using PLL(Phase locked loop) [7M]

SECTION – IV

7. a)Define i) Noise bandwidth ii) Noise figure [4M]

b) Derive the expression of figure of merit for Frequency modulated system. [10M]

(OR)

8. a) Derive the expression of figure of merit for SSBSC system.[10M]
   b) Explain about the noise temperature. [4M]

SECTION – V

9. a) Explain the characteristics of a radio receiver.[4M]
   b) Explain the operation of super hetero dyne receiver with the block diagram and mention its advantages and disadvantages. [10M]

(OR)

10. Explain the generation and demodulation of PPM signals.[10M]

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III B.Tech I Semester Regular Examinations

Analog Communications

(ECE)

Roll No										

Time: 3 hours Max. Marks: 70

Note: This question paper Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

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SECTION – I

14x5=70

1. a) Show, giving a mathematical proof, how a square-law device can be used to generate an AM signal. Give complete diagram of the signal input and output arrangements. Draw the output spectrum.[10M]

b) Explain the need for modulation.[4M]

OR

2. i)Explain Frequency Division Multiplexing with a neat diagram.[10M]

ii) Explain the need for VSB modulation.[4M]

SECTION – II

3. Find the percentage of power saved in SSB when compa red with AM system.[14M]

OR

4. a)Explain the method of Demodulation of an SSB-SC signal.[10M]

b) Discuss the advantages and disadvantages of SSB-SC transmission.[4M]

SECTION – III

5. Explain how a PLL can be used as an FM demodulator. [14M]

OR

6. a) Derive the expression for the FM signal under Tone Modulation and derive the expression its bandwidth.[10M]

b) Write a short note on transmission bandwidth of FM wave. [4M

SECTION – IV

7. Derive the canonical representation of the narrow band noise. Prove that both the in phase noise $n_c(t)$ and quadrature noise $n_s(t)$ have the same power spectral density.[14M]

OR

8. i)Derive the Noise figure & Equivalent noise temperature of a cascaded network.[8M]
ii) Define $(SNR)_O$, $(SNR)_C$, and figure of merit.[6M]

SECTION – V

9. Derive expressions of Signal to Noise Ratio for an DSB system using coherent demodulation.[14M]

OR

10. (a) Draw the block diagram of a Super Heterodyne receiver, and explain the operation of each stage of the receiver.[10M]

(b) A super Hetero dyne receiver is tuned to receive a 1000KHz carrier amplitude modulated by 1KHz sine wave. Assuming the IF of the receiver to be 455KHz, and the frequency components at the input and output of the IF amplifier. Assume the IF bandwidth to be 10 KHz. [4M]

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III B.Tech I Semester Regular Examinations

Analog Communications

(ECE)

Roll No										

Time: 3 hours Max. Marks: 70

Note: This question paper Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

SECTION – I

1. i) Explain the generation of Am wave using Switching Modulator.[10M]
ii) A carrier signal is sinusoidal modulated to a depth of μ=0.8. What is the percentage of the total power of the modulated signal is in the two sidebands?[4M]

OR

2. i)What are the different types of DSB-SC modulators? Explain them.[7M]
ii) Explain briefly the basic principle of FDM.[7M]

SECTION – II

3. i) Explain the detection of VSB signal using envelope detector.[10M]
ii) State the applications of VSB transmission. [4M]

OR

4. i)Derive the time domain expression for an SSB wave.[4M]
ii) Explain the generation of SSB modulated wave using Frequency discrimination Method. [10M]

SECTION – III

5. (a) Explain how PM signal can be generated from FM signal. Justify with the necessary mathematics and draw the block diagram of the corresponding implementation.[10M]

(b) For the FM signal $X(t) = 20.\text{Cos}[2\pi x10^6 t+2.\text{Sin}(2\pi x10^4 t)]$, plot the magnitude spectrum, as per Carson's rule. It is given that $J_0(2) = 0.224$; $J_1(2) = 0.577$; $J_2(2) = 0.353$; $J_3(2) = 0.129$. [4M]

OR

6. i) Explain how a Varactor Diode is used to generate FM signal. Explain with the necessary mathematical equations. [8M]
ii) Compare NBFM and WBFM. [6M]

SECTION – IV

7. i) Define $(SNR)_O$, $(SNR)_C$, and figure of merit.[6M]

ii)Prove that the cross-spectral densities of the quadrature components of narrow band noise are purely imaginary, as shown by

$$S_{NcNs}(f) = -S_{NcNs}(f) = \begin{cases} j[S_N(f+fc) - S_N(f-fc)]; & -B \le f \le B \\ 0 & \text{;elsewhere} \end{cases}$$.[8M]

OR

8. i)Derive the expression for Noise bandwidth.[7M]

ii)Write a short notes on white noise [7M]

SECTION – V

9. a) Explain the generation of PAM.[7M]

b) Explain the characteristics of Super heterodyne receivers.[7M]

OR

10. Explain FM receiver of the superheterodyne type.

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III B.Tech I Semester Regular Examinations

Analog Communications

(ECE)

Roll No										

Time: 3 hours Max. Marks: 70

Note: This question paper Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

SECTION – I

1. (a) Explain about the quadrature null effect of coherent detector.[6M]

(b) In DSB-SC, suppression of carrier so as to save transmitter power results in receiver complexity - Justify this statement. [8M]

OR

2. Explain the operation of an Envelope Detector. Explain about Diagonal Clipping in a diode detector. How to avoid it? [14M]

SECTION – II

3. a) State and prove the properties of Hilbert Transform of a Signal x(t).[7M]
b) Find the Hilbert Transform of [7M]

i. $x(t)=\text{sint}/t \cdot \cos 200\pi t$

ii. $x(t)=\text{sint}/t \cdot \sin 200\pi t$

OR

4. a)Derive the time domain expression of VSB wave. [6M]
b)Explain how a SSBSC signal is generated using phase shift method.[8M]

SECTION – III

5. For an FM Reactance Modulator, derive the expression for the: [14M]

a) Inductive reactance offered

b) Capacitive reactance offered.

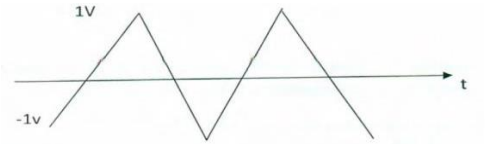
OR

6. a) A base band signal m(t) as shown below figure 1 modulates a sinusoidal carrier of frequency 100MHz, in its [7M]

i. phase

ii. Frequency.

The separation between the adjacent peaks of m(t) is 20mSec.The respective Phase sensitivity and Frequency sensitivity factors are 10π and $2\pi x10^5$. Find the Maximum and Minimum frequency in the corresponding FM and PM signals.



b) Justify that one form of Angle Modulation can be obtained from the other, with the necessary explanation. [7M]

SECTION – VI

7. Derive the Signal to noise ratios for coherent reception with SSB modulation.[14M]

OR

8 a)Define i) Noise bandwidth ii) Noise figure [4M]

b) Derive the expression of figure of merit for Frequency modulated system. [10M]

SECTION – V

9 (a) What is an Amplitude Limiter? Explain its operation with a neat circuit diagram. [7M]

(b) What is automatic gain control? What are its functions? [7M]

OR

10 (a) With the aid of the block diagram explain TRF receiver. List out the advantages and disadvantages of TRF receiver. [7M]

(b) Define and distinguish between PTM and PAM schemes. Sketch and explain their waveform for a single tone sinusoidal input signal. [7M]

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III B.Tech I Semester Regular Examinations

Analog Communications

(ECE)

Roll No										

Time: 3 hours Max. Marks: 70

Note: This question paper Consists of 5 SECTIONS (One SECTION for each UNIT). Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14marks.

SECTION – I

1. What is the necessity of synchronous Carrier in the coherent detection of a Suppressed carrier signal? Explain in detail, with the necessary mathematical treatment .[14M]

OR

2. Explain how an AM signal can be generated using Non-Linear Modulation, and derive the necessary equations.[14M]

SECTION – II

3. Explain the generation of SSB modulated wave using Frequency discrimination method.[14M]

OR

4. Explain the frequency description of VSB wave.[14M]

SECTION – III

5. Derive the expression for Wide band FM..[14M]

OR

6. Explain the operation of the balanced slope detector using a circuit diagram and draw its response characteristics. Discuss in particular the method of combining the outputs of the individual diodes. In what way is this circuit an improvement on the slope detector and in turn what are the advantages? .[14M]

SECTION – VI

7. (a) Derive the expression for the Figure of Merit for an envelope detector used to detect an AM-DSB-Full Carrier signal, under low noise case .[7M]

(b) An AM receiver operates with a tone modulation and the modulation index is 0.3. The message signal is 20.Cos1000πt. [7M]

i. Compute the figure of Merit.

ii. Determine the improvement in O/P signal to Noise Ratio if the modulation index is increased to 70%.

OR

8. Derive the expression for the Figure of merit for an FM receiver. [14M]

SECTION – V

9. (a) What is the fundamental difference between pulse modulation, on the one hand, and frequency and amplitude modulation on the other? .[7M]

(b) What is pulse width modulation? What other names does it have? How is it demodulated? .[7M]

OR

10. Describe the generation and demodulation of PPM with the help of block diagram and hence discuss its spectral characteristics.[14M]

R17A0417

INSTRUMENTATION ENGINEERING

Code No: R17A0417 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
III B.Tech I Semester
INSTRUMENTATION ENGINEERING
MODEL PAPER-I

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1. a) Explain the Performance characteristics of measurement system. [8M]
b) What is meant by D'Arsonval Movement .Explain about AC voltmeters in detail [6M]

OR

2. a) With a neat diagram explain in detail the construction of Multimeter. [7M]
b) What are the sources of errors? Explain the different types of errors in measurement? [7M]

SECTION-II

3. a) Discuss the working of Function generator with its basic circuit. [8M]
b) Explain with neat diagrams, the working of the RF Signal generator. [6M]

OR

4. a) Describe the working of a sweep frequency generator. [7M]
b) Explain the distortion analyzer with the help of suitable diagrams. [7M]

SECTION-III

5. a) Draw the block diagram of a CRO and explain the function of each block. [8M]
b) Explain block diagram of Dual Trace Oscilloscope with neat diagram. [6M]

OR

6. a)Draw the block diagram of CRT and explain each part. [7M]
b) Draw and explain about Sampling Oscilloscope with neat diagram. [7M]

SECTION-IV

7. a) Explain Bounded and unbounded wire strain gauges. [6M]
b) Explain the construction and operation of Thermocouples and write its applications. [8M]

OR

8. a) Explain the construction and operation principles of Linear Variable Differential Transformer (LVDT). [10M]
b) Explain Piezoelectric Transducers. [4M]

SECTION-V

9. a) Draw a circuit diagram of Wheat stone bridge and derive the equation for determining unknown quantities and also calculate current at unbalanced condition. [10M]

b) Write the applications of Kelvin bridge. [4M]

OR

10. a) Explain Data Acquisition system with neat diagram. [9M]

b) Explain the Measurement of Humidity and Moisture. [5M]

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Code No: R17A0417 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
III B.Tech I Semester
INSTRUMENTATION ENGINEERING
MODEL PAPER-II

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

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SECTION-I

1. a) With a neat diagram explain in detail the construction of DC voltmeter using PMMC Instrument. [8M]
   b) How do you measure large currents in PMMC (Ammeter) [6M]

OR

2. a) Explain the working of a true RMS voltmeter with the help of a suitable block diagram [8M]
   b) What are the sources of errors? Explain the different types of errors in measurement. [6M]

SECTION-II

3. a) With a neat diagram explain the working of Pulse and Square wave generator. [8M]
   b) Explain the working of Capacitance-Voltage meter. [6M]

OR

4. a) Discuss the working of spectrum analyzer with neat diagram. [8M]
   b) Explain the basic wave analyzer. [6M]

SECTION-III

5. a) Briefly explain the different types of storage oscilloscopes. [8M]
   b) What is the role of Time base generator? Explain. [6M]

OR

6. a) Explain dual trace oscilloscope with neat diagram. [10M]
   b) Explain how time and frequency is measured using CRO. [4M]

SECTION-IV

7. a) What are the factors to be considered for the selection of better transducer? [4M]
   b) Explain the principle and working of an LVDT. [10M]

OR

8. a) What is a transducer? Explain the working of Variable Capacitance transducer. [6M]
b) A 100Ω strain guage with a guage factor of 1 is affixed to a metal bar. The bar is stretched and this causes a change in resistance of 0.001Ω. Find the change in length if the original length is 10cm. [8M]

SECTION-V

9. a) With a neat diagram explain the working of Maxwell Bridge. [7M]

b) Explain the methods for the measurement of temperature. [7M]

OR

10.a) what are the different methods to measure liquid level and explain. [10M]

b) Discuss the principle of working of Displacement meters. [4M]

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Code No: R17A0417 **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
III B.Tech I Semester
INSTRUMENTATION ENGINEERING
MODEL PAPER-III

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

****

SECTION-I

1. a) Explain the block schematics of measurement system. [4M]
   b) what are different types of ohmmeters and Derive the equation for series type ohmmeter [10M]

OR

2. a) With a neat diagram explain in detail the construction of AC voltmter. [7M]
   b) What are the sources of errors? Explain the different types of errors in measurement? [7M]

SECTION-II

3. a) Discuss the working of frequency selective wave analyzer. [7M]
   b) Explain with neat diagrams, the working of the function generator. [7M]

OR

4. a) Describe the working of a sweep frequency generator. [7M]
   b) Explain the heterodyne wave analyzer with the help of diagram. [7M]

SECTION-III

5. a) Explain the CRO Probes. [7M]
   b) Explain block diagram of Dual beam Oscilloscope with neat diagram. [7M]

OR

6. a)Draw the block diagram of delay unit in CRO and explain each part. [7M]
   b) Draw and explain about Sampling Oscilloscope with neat diagram. [7M]

SECTION-IV

7. a) Explain the hotwire anemometer. [7M]
   b) Explain the construction and operation of Resistance Thermometer and write its applications. [7M]

OR

8. a) Explain the construction and operation principles of Linear Variable Differential Transformer(LVDT). [10M]

b) Explain Piezoelectric Transducers. [4M]

SECTION-V

9. a) Explain the measurement of Velocity. [7M]

b) Explain the Measurement of Humidity and Moisture. [7M]

OR

10. a) Explain the measurement of vacuum pressure. [14M]

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Code No: **R17A0417** **R17**

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

III B.Tech I Semester

INSTRUMENTATION ENGINEERING

(ECE)

MODEL PAPER-IV

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: This question paper Consists of 5 Sections. Answer **FIVE** Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

****

SECTION – I

1. a) List different types of measuring instruments and Give the block schematic of a general measuring system and explain. [10M]

b) Explain RF ammeter. [4M]

(OR)

2. a) Explain the static and dynamic characteristics of an instrument. [7M]

b) What are the different types of errors in measurement? Explain. [7M]

SECTION – II

3. a) Describe the working of Heterodyne wave analyzer with the block diagram [7M]

b) Describe the working of a pulse and square wave generator. [7M]

(OR)

4. a) Describe the working of a sweep frequency generator. [7M]

b) Explain the distortion analyzer with the help of suitable diagrams. [7M]

SECTION – III

5. a) By lissajous pattern method, explain how the phase difference between two sinusoidal signals can be measured [8M]

b) Explain Time base circuit in CRO [6M]

(OR)

6. a). Draw the block diagram of a CRO and explain the function of each block. [7M]

b) Explain block diagram of Dual Trace Oscilloscope with neat diagram **[7M]**

SECTION – IV

7. a) Explain Bounded and unbounded wire strain gauges. [8M]

b) Explain the construction and operation of Thermocouples and write its applications.. [6M]

(OR)

8. a) Explain the construction and operation of Linear Variable differential Transducer. [10M]

b) Explain Piezoelectric Transducers. [4M]

SECTION – V

9. a) Draw a circuit diagram of Wheat stone bridge and derive the equation for determining unknown quantities and also calculate current at unbalanced condition. [10M]

b) Explain the measurement of Flow. [4M]

(OR)

10.a) In the case of Maxwell's bridge, one arm has resistance of 1K Ω, in another arm has also only resistance of 5K Ω. The third arm has a resistor 4-7k Ω in shunt with a capacitor of 1μF. The bridge is excited at frequency of 1KHz.Determine the Values of an unknown Lx in the fourth arm. [10M]

b) Explain the measurement of Humidity [4M].

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R17A0410
Digital Design Through Verilog

R17

Code No: R17A0410

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
III B. Tech I Semester Model Paper-1
Digital Design Through Verilog
(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1. a) Explain different levels of design description in Verilog. **[7M]**
   b) Explain about keywords, Identifiers and white space characters. **[7M]**

OR

2. Define the terms relevant to Verilog HDL. **[14M]**
   (i) Simulation
   (ii) PLI
   (iii) System tasks

SECTION-II

3. Write short notes on the following with examples. **[14M]**
   (i) Logical operators
   (ii) Conditional operator
   (iii) Arithmetic operators

OR

4. Explain about tri-state buffers and describe using Verilog module. **[14M]**

SECTION-III

5. Explain blocking and Non-blocking statements with examples. **[14M]**

OR

6. a) Explain about initial and always constructs. **[7M]**
   b) Design a 4:1 Mux using case statement. **[7M]**

SECTION-IV

7. a) Describe the basic transistor switches in detail? **[7M]**
   b) Discuss about Path Delays in detail? **[7M]**

OR

8 a) Design a 3 input CMOS NAND gate. Write the Verilog code and test bench for it. **[7M]**
   b) Explain about basic transistor switches. **[7M]**

SECTION-V

9. a) What is the importance of user defined primitives? Explain. **[6M]**
   b) Implement RAM cell using CMOS switch and describe it using Verilog. **[4M]**

OR

10. Explain about compiler directives and path delays in Verilog **[14M]**

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R17

Code No: R17A0410

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
III B. Tech I Semester Model Paper-21
Digital Design Through Verilog
(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1. a) Discuss about Programming Language Interface. **[3+4M]**
   b) Explain module with suitable example.
   c) Explain the following Verilog HDL operators? **[7M]**
      i) Unary operator
      ii) Binary operator
      iii) Ternary operator

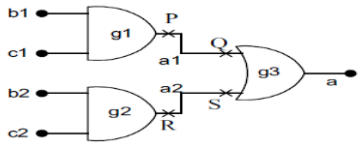
OR

2. a) Explain about the following **[7M]**
   i) Verilog as HDL
   ii) Concurrency
   b)Explain the Data types with simple programs relevant to the data types **[7M]**

SECTION-II

3. Describe Gate Delays? Write the Verilog HDL code for following schematic diagram. Assume the following conditions. Rise Time Delay is "2" and Fall Time Delay is "1" for wires a1,a2; **[14M]**

Rise Time Delay is "3" and Fall Time Delay is "4" for g1;
Rise Time Delay is "5" and Fall Time Delay is "6" for g2;
Rise Time Delay is "8" and Fall Time Delay is "7" for g3;



OR

4. a) Implement 8:1 Mux using 4:1 Mux & 2:1 Mux and write the Verilog HDL code? **[7M]**
   b) Discuss about the equality operators in detail with examples. **[7M]**

SECTION-III

5. a) Design a Priority Encoder circuit using casex concept **[7M]**
   b) Explain the concept of Multiple always constructs? **[7M]**

OR

6. a) Distinguish between Sequential Block (begin-end) and Parallel Block (fork-join) with **[7M]**

examples?

b) Design a 4:1 Mux using if-else construct? **[7M]**

SECTION-IV

7. a) Describe the basic transistor switches in detail? **[7M]**

   b) Discuss about Path Delays in detail? **[7M]**

OR

8 a) Prepare a verilog module to design a 1-bit RAM cell **[7M]**

b)Write a UDP to design posedge triggered D flip-flop with asynchronous set and reset **[7M]**

SECTION-V

9. a)What are the basic Sequential models explain with its relevant diagrams **[6M]**

   b) Write the verilog code for Universal Shift Register **[4M]**

OR

10. a) Discuss about the assertion verification in detail using assertion monitors with suitable examples. **[10M]**

    b) Explain the flip-flop timing with suitable examples **[4M]**

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R17

Code No: R17A0410

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
III B. Tech I Semester Model Paper-3
Digital Design Through Verilog
(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1. a) Explain the simulation and synthesis in Verilog HDL. **[7M]**
   b) Explain the concept of numbers in language constructs. **[7M]**

OR

2. a) Explain the components of a Verilog module. **[10M]**
   b) Define keywords and Identifiers. **[4M]**

SECTION-II

3. a) Classify and explain strengths and contention resolution. **[8M]**
   b) Write Verilog code for RS latch and test bench. **[6M]**

OR

4. a) Describe module structure with an example. **[7M]**
   b) Design 3 to 8 decoder using gate level design description **[7M]**

SECTION-III

5. a) Explain with an example how while construct used. **[7M]**
   b) Explain case statement with suitable Verilog module. **[7M]**

OR

6. a) Design an 8-bit adder module using for loop. **[7M]**
   b) Explain disable construct with an example. **[7M]**

SECTION-IV

7. a) Describe the bi-directional transistor switches in detail? **[7M]**
   b) Explain time delays with switch primitives. **[7M]**

OR

8 a) Design a 2 input CMOS NOR gate. Write the Verilog code and test bench for it. **[8M]**
   b) Explain about CMOS switches. **[6M]**

SECTION-V

9. a) Define parameter? Explain defparam and specparam. **[6M]**
   b) Explain the sequential Model –feedback Model **[4M]**

OR

10. What are the system tasks available in Verilog and explain with suitable module. **[14M]**

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R17

Code No: R17A0410

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
(Autonomous Institution – UGC, Govt. of India)
III B.Tech I Semester Model Paper-4
Digital Design Through Verilog
(ECE)

Roll No										

Time: 3 hours **Max. Marks: 70**

Note: Answer FIVE Questions, Choosing ONE Question from each SECTION and each Question carries 14 marks.

SECTION-I

1. a) What are the system tasks available in Verilog for making and controlling simulation? **[3M]**
   b) Write the structure of typical simulation module and explain. **[7M]**
   c) Define Scalars and Vectors. **[4M]**

OR

2. a) Write Short notes on functional verification. **[4M]**
   b) Explain about the following **[10M]**
   (i) Numbers
   (ii) Data types

SECTION-II

3. a) Write gate level module and test bench for Clocked SR flip flop. **[7M]**
   b) Explain 'wand' and 'wor' types of nets with examples. **[7M]**

OR

4. a) Explain in detail net, gate and tri-state delays with examples and Verilog code? **[7M]**
   b) Write Verilog module for 8-bit comparator with test bench. **[7M]**

SECTION-III

5. a) Design a 2:4 demultiplexer module and test bench using the if-else-if construct in a Verilog. **[7M]**
   b) Write Short notes on **[7M]**
   (i) Functional Bifurcation.
   (ii) Intra-assignment delays

OR

6. a) Design a counter module and test bench to illustrate the use of WAIT construct in a Verilog. **[7M]**
   b) What are the advantages of multiple always block. Explain with example. **[7M]**

SECTION-IV

7.	a) Differentiate between regular and resistive switches in Verilog.	**[7M]**
	b) Discuss about Path Delays in detail?	**[7M]**
	OR	
8	a) Write a Verilog design description module of a CMOS NOR gate.	**[7M]**
	b) Explain how instantiation is done with 'Strengths' and 'Delays'.	**[7M]**

SECTION-V

9.	a) Design a Gray Code Counter and write its Verilog code.	**[6M]**
	b) Write notes on different sequential models.	**[8M]**
	OR	
10.	a) Write notes on compiler directives and user defined primitives.	**[10M]**
	b) Write module of a D-latch using non-blocking assignments.	**[4M]**

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R17A0507

INTRODUCTION TO JAVA PROGRAMMING

R17

Code No: xxxxxxx

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

QUESTION PAPER

INTRODUCTION TO JAVA PROGRAMMING

Roll No										

Time: 3 hours **Max. Marks: 70**

Note:

Question paper Consists of 5 SECTIONS (One SECTION for each UNIT).
Answer **FIVE** Questions, Choosing **ONE** Question from each SECTION and each Question carries 14 marks.

SECTION-I

1). Explain briefly about Object Oriented Programming concepts? [14M]

(OR)

2. a) Explain briefly about type conversion and type casting with example program? [7M]

b) Write a java program for finding the factorial of a given number using recursion? [7M]

SECTION-II

3. a)Explain different types of inheritances with example program? [7M]

b)What is a package? Explain User defined package with program? [7M]

(OR)

4. a)Explain method overriding with example program? [7M]

b) Explain super keyword with program? [7M]

SECTION-III

5. a) What is an Exception? Explain different types of Exceptions? [7M]

b) Explain about try and catch with example program? [7M]

(OR)

6 a) Explain how to create a Thread with example program? [7M]

b) Explain about Thread Synchronization with program? [7M]

SECTION- IV

7). What is an Applet? Explain Applet life Cycle with neat diagram [14M]

(OR)

9. a)Explain FileInputStream and FileOutputStream with program? [7M]

b) Write a program for Handling Mouse Events? [7M]

SECTION- V

10.a) Explain about AWT class hierarchy? [7M]

b**)** Explain about AWT and Swing? [7M]

(OR)

11) Explain different types of Layouts with example program? [14M]

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R17

Code No: xxxxxxx

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

QUESTION PAPER

INTRODUCTION TO JAVA PROGRAMMING

Roll No										

Time: 3 hours **Max. Marks: 70**

Note:

Question paper Consists of 5 SECTIONS (One SECTION for each UNIT).

Answer **FIVE** Questions, Choosing **ONE** Question from each SECTION and each Question carries 14 marks.

SECTION-I

1) Explain Procedure oriented programming and Object Oriented programming? [14M]

(OR)

2. a) Explain different loop control statements with example program? [7M]

b) Explain parameter passing Mechanism with example program? [7M]

SECTION-II

3. a) Explain Method overriding and Abstract class with example program? [7M]

b) What is an Interface? Explain how to extend one interface with another [7M]

(OR)

4. a)Difference between Interface and Abstract class? [7M]

b) Explain final keyword with method and class? [7M]

SECTION-III

5. a) Explain about checked and unchecked Exceptions in java? [7M]

b) Explain finally block with example program? [7M]

(OR)

6 a) What is a Thread? Explain Thread Life cycle with neat diagram? [7M]

b) Explain Inter-Thread Communication with Producer and Consumer problem? [7M]

SECTION- IV

7) Explain differences between Applet and Application? [14M]

(OR)

9. a) Explain Event classes and Event Listeners with example? [7M]

b) Write a program for handling Key Events? [7M]

SECTION- V

10.a) Explain about Graphic class methods? [7M]

b**)** Explain about Border, Grid, and Flow Layouts in java? [7M]

(OR)

11) Explain about AWT controls with program? [14M]

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R17

Code No: xxxxxxx

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

QUESTION PAPER

INTRODUCTION TO JAVA PROGRAMMING

Roll No										

Time: 3 hours **Max. Marks: 70**

Note:

Question paper Consists of 5 SECTIONS (One SECTION for each UNIT).

Answer **FIVE** Questions, Choosing **ONE** Question from each SECTION and each Question carries 14 marks.

SECTION-I

1). Explain Constructor Overloading and Method Overloading with example program? [14M]

(OR)

2. a) Explain different Operators in Java with examples [7M]

b) Explain about Scanner and StringTokenizer class? [7M]

SECTION-II

3. a)Explain Dynamic binding with example program? [7M]

b)What is an interface? Explain how to extend an interface with program? [7M]

(OR)

4. a)Explain different Access Specifiers in java? [7M]

b) Explain about this keyword and built in packages? [7M]

SECTION-III

5. a) Explain throw and throws keyword with example program? [7M]

b)Explain nested try block with example program? [7M]

(OR)

6 a) Explain Thread Synchronization with example program? [7M]

b) Explain about Creating a Thread with program ? [7M]

SECTION- IV

7). Explain FileInputStream with program? [14M]

(OR)

9. a)Write a program for handling Mouse Events? [7M]
b) Explain Adapter class with example program? [7M]

SECTION- V

10.a) Differences between AWT and Swings? [7M]

b**)** Difference between Applets and Applications? [7M]

(OR)

11) Explain about Layout Managers with program [14M]

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R17

Code No: xxxxxxx

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

QUESTION PAPER

INTRODUCTION TO JAVA PROGRAMMING

Roll No										

Time: 3 hours **Max. Marks: 70**

Note:

Question paper Consists of 5 SECTIONS (One SECTION for each UNIT).

Answer **FIVE** Questions, Choosing **ONE** Question from each SECTION and each Question carries 14 marks.

SECTION-I

1). Explain about Java Buzz words or Features and History of java [14M]

(OR)

2. a) Explain about Garbage Collector in java ? [7M]

b) Explain this keyword with example program? [7M]

SECTION-II

3. a)Explain different types of inheritances in java? [7M]

b)Explain difference between Abstract class and Interface? [7M]

(OR)

4. a)Explain about super keyword with example program? [7M]

b) Explain how multiple inheritance is supported in java? Justify [7M]

SECTION-III

5. a) What is Exception? Explain Built in Exceptions in java [7M]
b)What is Built in Exceptions in java [7M]

(OR)

6 a) Explain about Thread Synchronization with program? [7M]

b) Explain Inter Thread Communication with program? [7M]

SECTION- IV

7). Explain FileOutputStream with program? [14M]

(OR)

9. a) Explain different types of applets in java [7M]
b) Explain how to pass parameters to an applet with program? [7M]

SECTION- V

10.a) Explain about Delegation Event Model? [7M]

b**)** Difference between AWT and Swing [7M]

(OR)

11) Explain AWT components [14M]
i) Label ii) Button iii) Text Field iv) Checkbox

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R17A0569

Computer Organization & Operating Systems

R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

B.Tech III year – I Semester Examinations, Model Paper-I

Computer Organization & Operating Systems

(ECE)

Time: 3 hours

Answer one question from each section. **Max. Marks: 70**

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SECTION – I

1. a) Explain the following with neat sketches:
   i) 4 – bit Binary adder ii) Binary Adder – Subtractor (7M)
   b) Explain how registers are connected to common bus in the computer with a neat diagram. (7M)

(OR)

2. a) Explain 4-bit binary incrementer with a neat diagram (7M)
   b) Find 2's complement of the following (7M)
   (i) 10010 ii) 111000 iii) 0101010 iv) 111111

SECTION – II

3. Discuss the design of control unit. (14M)

(OR)

4. Discuss the memory mapping functions to place memory blocks in the cache. (14M)

SECTION – III

5. a)Why does DMA have priority over the CPU When both request a memory transfer? (8M)
   b) Discuss asynchronous data transfer. (6M)

(OR)

6. What is the difference between isolated IO and memory mapped I/O? State the advantages and disadvantages of each. (7M)
7. What is a DMA controller? Explain. (7M)

SECTION – IV

8. a) Write about deadlock conditions and bankers algorithm in detail. (8M)
   b) What is a page fault? Explain the steps involved in handling a page fault with a neat sketch. (6M)

(OR)

9. a) How does deadlock avoidance differ from deadlock prevention? Write about deadlock avoidance algorithm in detail. (8M)
   b) What are the disadvantages of single contiguous memory allocation? Explain. (6M)

SECTION – V

10. a) Explain directory implementation. (7M)
    b) Discuss contiguous allocation of disk space. (7M)

(OR)

11. a) Explain a typical file control block. (7M)
    b) Illustrate and discuss linked allocation of disk space with a neat diagram. (7M)

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R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

B.Tech III year – I Semester Examinations, Model Paper-II

Computer Organization & Operating Systems

(ECE)

Time: 3 hours **Max. Marks: 70**

Answer one question from each section

SECTION – I

1 .a) Perform the following: (4)

(i) $(110.101)_2 = (\ )_{10}$

(ii) $(1.10101)_2 = (\ )_{10}$

(iii) $(11010.1)_2 = (\ )_{10}$

(iv) 110.10 x 10.1

b) Write sixteen logic microoperations. (5)

c)Discuss about fixed point representation. (5)

(OR)

2 a) Explain shift microoperations. (5)

b) Distinguish between error detection and error correction. Explain with an example how Hamming code is used for error detection. (5)

c) Draw the memory hierarchy in a computer system. (4)

SECTION – II

3.a) Mention the advantages and disadvantages of microprogrammed control hardwired control. (10)

b) List the address sequencing capabilities required in a control memory. (4)

(OR)

4.a) Discuss asynchronous DRAMs and synchronous DRAMs. (10)

b) Distinguish between Logical and Physical address space. (4)

SECTION – III

5.a) How the data transfer to and from peripherals is done? Discuss with neat diagrams and examples. (10)

b) Discuss source initiated transfer using handshaking. (4)

(OR)

6.What is a DMA controller? Explain. (14)

SECTION – IV

7.a) What is a deadlock? How deadlocks are detected? (5)
b)What is demand paging? (3)
b) What is a Virtual Memory? Discuss the benefits of virtual memory technique.(6)

(OR)

8.a) Explain the Resource Allocation Graph algorithm for deadlock avoidance. (8)
b) What is the cause of Thrashing? How does the system detect Thrashing? What can the system do to eliminate this problem? (6)

SECTION – V

12. a) Explain the layered file system. (5)
b) What are the various attributes that are associated with an opened file? (3)
c) Discuss schematic view of a file system. (6)

(OR)

11.a) Explain the various methods for free-space management. (5)
b) Discuss virtual file system. (2)
b) Illustrate and discuss indexed allocation of disk space with a neat diagram. (5)

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R17

MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

B.Tech III year – I Semester Examinations, Model Paper-III

Computer Organization & Operating Systems

(ECE)

Time: 3 hours

Answer one question from each section. **Max. Marks: 70**

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SECTION – I

1. a) What are the functional units of a computer? Explain the Bus Structures in detail? 8M

b) Describe about shift micro operations. 6M

OR

2. a) Describe about stack organization. 7M

b) List and explain different performance measures used to represent a computer system Performance. 7M

SECTION – II

3. a) Explain the functioning of a micro-programmed control unit with a neat diagram? 7M

b) Write a short note on RAM memory. 7M

OR

4. Hardwired control unit is faster than micro-programmed control unit. Justify this statement. 14M

SECTION – III

5. Explain various registers in DMA interface with their purpose 14M

OR

6. Write a short note on the following 14M

a) USB b) IEE1394 c) Input Output devices d) RS232

SECTION – IV

7. a) Explain the difference between internal and external fragmentation. 7M

b) Discuss Characteristics of deadlock 7M

OR

8. a) What is paging explain any one of the paging technique with suitable example? 8M

b) Write a short note on structure of operating system and system calls 7M

SECTION – V

9. Explain the following terms with neat diagrams and examples:

a) Two level directory structure. 7M

b) DAG structure. 7M

OR

10. Explain the concept of free space management?
14M

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MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

(Autonomous Institution – UGC, Govt. of India)

B.Tech III year – I Semester Examinations, Model Paper-IV

Computer Organization & Operating Systems

(ECE)

Time: 3 hours

Answer one question from each section. **Max. Marks: 70**

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SECTION – I

1. a) a) Illustrate the basic Operational concepts of a computer with a neat diagram? 7M

b) Describe about Arithmetic Logic Shift Unit. 7M

OR

2. a) Represent 1259.125_{10} in single precession and double precession formats? 7M

b) List and explain different addressing modes? 7M

SECTION – II

3. a) Give the micro instruction format? Explain 7M

b) Discuss briefly about virtual memory 7M

OR

4. a)**.** Draw and explain hardwired control unit? 7M

b) Compare and contrast direct and associative techniques 7M

SECTION – III

5. What is interrupt? What are the types of interrupts explain the purpose of interrupt handler 15M

OR

6. Write a short note on (4+4+6)M

a) Programmed I/O

b) Interrupt driven I/O

c) DMA Controller

SECTION – IV

7. a) Explain the concept of Protection and security in operating systems? 7M

b) What is segmentation? Explain 7M

OR

8. a) What is dead lock Explain dead lock prevention mechanism 7M

b) Explain about the implementation of the hashed page table approach. 7M

SECTION – V

9. a) Explain how the remote file sharing can be done in RFS 7M

b) Explain different File Accessing methods 7M

OR

10. Write short notes on (4 + 4 + 7)M

a) File sharing b) file protection c) File System Implementation